A Scalable Architecture of a Structured LDPC Decoder[1]

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Abstract — **We present a scalable decoding architecture for a certain class of structured LDPC codes. The codes are designed using a small (n, r) protograph that is replicated Z times to produce a decoding graph for a $(Z \times n, Z \times r)$ code. Using this architecture, we have implemented a decoder for a $(4096, 2048)$ LDPC code on a Xilinx Virtex-II 2000 FPGA, and achieved decoding speeds of 31 Mbps with 10 fixed iterations. The implemented message-passing algorithm uses an optimized 3-bit non-uniform quantizer that allows near floating point performance in the waterfall region, with drastically smaller hardware implementation requirements.**

I. Structured LDPC Decoder Architecture

We developed an architecture for decoding structured LDPC codes in which computations are scheduled in space and time. A structured LDPC code is constructed from a small (n, r) protograph[1] by making Z copies of each variable and check node. Each edge in the small protograph represents a set of edges in the larger code graph which connect Z copies of a variable node with Z copies of a check node via an arbitrary permutation (see figure 1).

In our hardware architecture, we instantiate hardware units for each of the n variable nodes and r check nodes in the small LDPC protograph. All n variables node units or all r check node units decode synchronously and in parallel. The Z copies of the identical small protograph share this hardware and are operated on serially. Messages are stored in memory modules, each of which corresponds to an edge in the small protograph.

The cornerstone of our hardware architecture is the scheduling of message-updates in space and time. One iteration consists of a check node phase, followed by a variable node phase. In each phase, there are Z computation cycles to update the Z messages in each edge memory.

II. Quantized Belief Propagation Algorithm

We use a non-uniform quantization scheme optimized for regular $(3, 6)$ LDPC codes. Compared to the full floating point simulation done in software, hardware 3-bit non-uniform quantization is only off about 0.2 dB, with drastically smaller hardware implementation requirements. Benefiting from the small hardware requirement for each processing unit, many more processing units can be put in one FPGA to decode a much bigger codeword, thus improving the error-correcting capability.

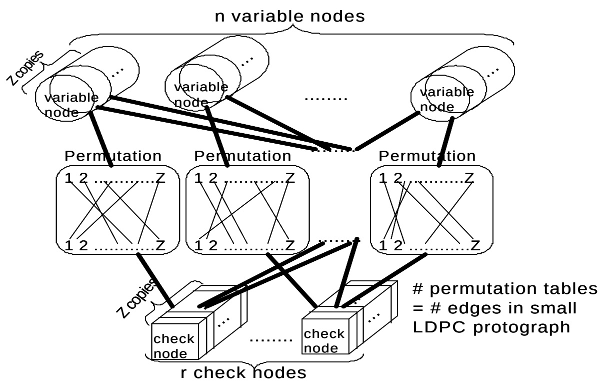

Figure 1: Structured LDPC decoder architecture

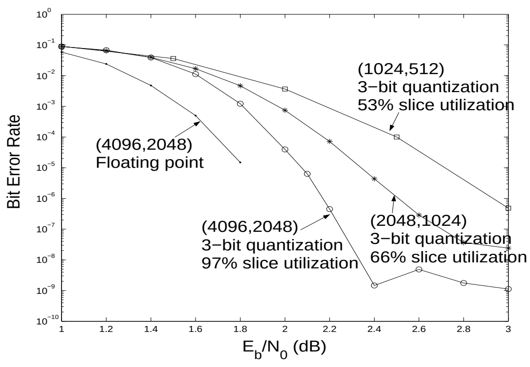

Figure 2: Performance/FPGA Area at varying block size

III. Performance

Using our scalable decoder architecture, we implemented several codes of different block lengths, and ran performance tests to compare their performance differences. The largest block length code we can implement on a Xilinx Virtex-II 2000 FPGA chip is a $(32, 16) \times 128$ copies $= (4096, 2048)$ code. The results demonstrate that doubling the block length can improve the performance by about 0.5 dB (see figure 2).

The decoder throughput depends on two factors: communication overhead and decoder speed. Decoder speed is proportional to the number of iterations. The measured decoder speed is 3.18 ns/bit/iteration. The measured communication overhead is 97.1 ns/bit in our tests. Communication overhead includes the buffer delay outside the decoder module, and the time delay writing to and reading from the FPGA board. Therefore, at 10 iterations, decoding speed is 31 Mbps without communication overhead or 8 Mbps with communication overhead.

References

[1] J. Thorpe, “Low-Density Parity-Check (LDPC) Codes Constructed from Protographs,” *IPN Progress Reports 42-154*, April-June 2003.

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